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1 **Implementation of 13 kbps QCELP vocoder ASIC**
Kyung-Jin Byun; Minsoo Hahn; Kyung-Su Kim;
ASICs, 1999. AP-ASIC '99. The First IEEE Asia Pacific Conference on , 23-25 A 1999
Pages:258 - 261

[Abstract] [PDF Full-Text (340 KB)] **IEEE CNF**

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2 **A 150 MIPS/W CMOS RISC processor for PDA applications**
Nagamatsu, M.; Tago, H.; Mijamori, T.; Kamata, M.; Murakami, H.; Ootaguro, Goto, H.; Utsumi, T.; Teruyama, T.; Mabuchi, K.; Kawasumi, A.; Malik, K.;
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Pages:114 - 115, 347

[Abstract] [PDF Full-Text (688 KB)] **IEEE CNF**

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3 **A 1.2 W 66 MHz superscalar RISC microprocessor for set-tops, video games, and PDAs**
Dac Pham; Kahle, J.; Ogden, D.; Putrino, M.; Tai Ngo; Hoover, K.; Cang Tran; Sweet, M.; Hung Hua; Quan Nguyen; Mallick, S.; Eisen, L.; Loper, A.; Chitturi Lyon, T.; Ho, B.; Patel, R.; Cheesebrough, E.; Kuttanna, B.; Piejko, A.;
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[Abstract] [PDF Full-Text (868 KB)] **IEEE CNF**

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4 **A mixed-signal 0.18-µm CMOS SoC for DVD systems with 432-MSample/s PRML read channel and 16-Mb embedded DRAM**

Yamamoto, T.; Gotoh, S.-I.; Takahashi, T.; Irie, K.; Ohshima, K.; Mimura, N.;
Solid-State Circuits, IEEE Journal of , Volume: 36 , Issue: 11 , Nov. 2001
Pages:1785 - 1794

[Abstract] [PDF Full-Text (427 KB)] **IEEE JNL**

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5 **A 1.2-W, 2.16-GOPS/720-MFLOPS embedded superscalar microproce for multimedia applications**
Kubosawa, H.; Takahashi, H.; Ando, S.; Asada, Y.; Asato, A.; Suga, A.; Kimur M.; Higaki, N.; Miyake, H.; Sato, T.; Anbutsu, H.; Tsuda, T.; Yoshimura, T.; Amano, I.; Kai, M.; Mitarai, S.;
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Pages:1640 - 1648

[Abstract] [PDF Full-Text (196 KB)] **IEEE JNL**

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6 **A 433-MHz 64-b quad-issue RISC microprocessor**
Gronowski, P.E.; Bowhill, W.J.; Donchin, D.R.; Blake-Campos, R.P.; Carlson, D Equi, E.R.; Loughlin, B.J.; Mehta, S.; Mueller, R.O.; Olesin, A.; Noorlag, D.J.W Preston, R.P.;
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Kever, W.; Ziai, S.; Hill, M.; Weiss, D.; Stackhouse, B.;
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9 **A microinstrumentation system for industrial applications**
Higino Correia, J.; Cretu, E.; Bartek, M.; Wolffenbuttel, R.F.;
Industrial Electronics, 1997. ISIE '97., Proceedings of the IEEE International Symposium on , 7-11 July 1997
Pages:846 - 850 vol.3

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Montanaro, J.; Witek, R.T.; Anne, K.; Black, A.J.; Cooper, E.M.; Dobberpuhl, D Donahue, P.M.; Eno, J.; Farell, A.; Hoeppner, G.W.; Kruckemyer, D.; Lee, T.H Lin, P.; Madden, L.; Murray, D.; Pearce, M.; Santhanam, S.; Snyder, K.J.; Stephany, R.; Thierauf, S.C.;

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11 **An implementation of an embedded microprocessor core with suppo for executing byte compiled Java code**
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Digital Systems, Design, 2001. Proceedings. Euromicro Symposium on , 4-6 S 2001
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[Abstract] [PDF Full-Text (376 KB)] IEEE CNF

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1 **Vector instruction set support for conditional operations**
Smith, J.E.; Faanes, G.; Sugumar, R.;
Computer Architecture, 2000. Proceedings of the 27th International Symposiu on , 10-14 June 2000
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1 **Sequential logic optimization for low power using input-disabling precomputation architectures**
Monteiro, J.; Devadas, S.; Ghosh, A.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 17 , Issue: 3 , March 1998
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[Abstract] [PDF Full-Text (164 KB)] **IEEE JNL**